Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A computer system, comprising:

a processor ~~which includes~~that comprises a hardware branch predictor; and

~~a program of~~ software instructions executed by said processor, said software instructions ~~including~~ comprising conditional branch instructions and separate static branch prediction instructions;

said static branch prediction instructions ~~include~~ comprise a plurality of groups of static branch prediction bits, each group being configurable to provide prediction information for ~~which correspond to~~ a separate conditional branch instructions.

2. (Canceled).

3. (Canceled).

4. (Currently Amended) The computer system of claim 21, wherein each group of static branch prediction bits comprises a pair of bits~~said static branch prediction bits included in a static branch prediction instruction include pairs of prediction bits, each pair providing prediction information for a separate instruction in said group of n other instructions~~.

5. (Currently Amended) The computer system of claim [[4]]1 wherein said prediction information ~~includes~~ comprises a member selected from the group consisting of: do not use static prediction, predict taken, and predict not taken.

6. (Original) The computer system of claim 4 wherein each pair of prediction bits corresponds to another instruction and each pair of prediction bits is encoded as: 00 and 01 mean do not use static prediction, 10 means predict taken and 11 means predict not taken.

7. (Currently Amended) The computer system of claim 1 wherein said static branch prediction bits ~~include~~ comprise static branch prediction information that ~~includes~~ comprises encoded information directing the processor to ignore the predictions supplied by the hardware branch predictor.

8. (Currently Amended) The computer system of claim 1 wherein said hardware branch predictor ~~includes~~ comprises a log in which the results of all executed conditional branch instructions are stored.

9. (Currently Amended) A processor, comprising:

fetch logic that fetches program instructions from a source external to said processor;

a dynamic branch predictor coupled to said fetch logic, said dynamic branch predictor supplies predictions regarding conditional branch instructions to said fetch logic;

an instruction queue coupled to said dynamic predictor, said fetch logic storing fetched instructions in said instruction queue; and

an execution unit coupled to said instruction queue and executing instructions provided from said instruction queue;

said fetch logic examines fetched instructions for a predetermined register identifier that identifies that instruction as a static branch prediction instruction that provides separate static branch prediction information about ~~other fetched instructions~~a plurality of conditional branch instructions.

10. (Canceled).

11. (Canceled).

12. (Currently Amended) The computer system of claim 10, wherein said separate static branch prediction information for each conditional branch instruction comprises a pair of bits ~~prediction bits included in a static branch prediction instruction include a plurality of pairs of prediction bits, each pair providing prediction information for a separate instruction in said group of n other instructions~~.

13. (Currently Amended) The processor of claim ~~12~~ 9 wherein said prediction information ~~includes~~ comprises a member selected from the group consisting of: do not use static prediction, predict taken, and predict not taken.

14. (Canceled).

15. (Currently Amended) The processor of claim 9 wherein said static branch prediction instruction ~~includes~~ comprises branch prediction bits ~~which encodes information directing~~that directs said fetch logic to ignore the predictions supplied by the dynamic branch predictor.

16. (Currently Amended) The processor of claim 9 wherein said dynamic branch predictor ~~includes~~ comprises a log in which the results of all executed conditional branch instructions are stored.

17. (Original) The processor of claim 9 wherein said predetermined identifier comprises a register identifier.

18. (Currently Amended) A method of predicting the outcome of conditional branch instructions, comprising:

~~(a)~~ including a static branch predictor software instruction in a program, said branch prediction software instruction including branch

prediction information configurable to pertaining to a plurality of conditional branch other instructions in the program;

(b) fetching said branch prediction software instructions;

(c) decoding said branch prediction software instructions to determine if said decoded instruction is a branch prediction software instruction; and

(d) if said decoded instruction is a branch prediction software instruction, then using said branch prediction information for branch prediction.

19. (Canceled).

20. (Canceled).

21. (Currently Amended) The method of claim 18 wherein said branch prediction information includes comprises pairs of bits, each pair corresponding to another one of said other instructions.

22. (Currently Amended) The method of claim 21 further including comprising decoding said pairs of bits to determine whether, for said other instruction corresponding to said pair, said other instruction is predicted taken, predicted not taken or no static branch prediction is provided.